In the Claims

RULE 1.126 Please cancel claims 1-19. Please add the following claims:

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~~20.~~ Volume control circuitry for controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer is configured to provide a volume component to wavetable data addressed by said synthesizer, comprising:

(a) a memory having a first storage location configured to store a current value of said volume component, and a second storage location configured to store a final value of said volume component, wherein said final value is directly programmed into said second storage location;

(b) a comparator coupled to said memory for periodically comparing said current value with said final value to determine if said current value is less than, greater than, or equal to said final value; and

(c) an incrementor coupled to said comparator and said memory, wherein said incrementor is configured to increment said current value in response to a determination by said comparator that said current value is less than said final value, and configured to decrement said current value in response to a determination by said comparator that said current value is greater than said final value.

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~~21.~~ The volume control circuitry of claim 20, wherein said first and second storage locations are registers.

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~~22.~~ The volume control circuitry of claim 20, wherein when said incrementor increments or decrements said current value, said increment or decrement is by a value of one.

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~~23.~~ Volume control circuitry for controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer interfaces and provides audio enhancement to a host computer of the type including a central processor, and wherein

said synthesizer is configured to provide a volume component to wavetable data addressed by said synthesizer, comprising:

(a) a first storage device for storing a current value of said volume component;

(b) a second storage device configured to store a final value of said volume component, wherein said final value is programmed into said second storage device by the central processor;

(c) a comparator coupled to said first and second storage devices for periodically comparing said current value with said final value to determine if said current value is less than, greater than, or equal to said final value; and

(d) an incrementor coupled to said comparator and said first storage device, wherein said incrementor is configured to increment said current value in response to a determination by said comparator that said current value is less than said final value, and configured to decrement said current value in response to a determination by said comparator that said current value is greater than said final value.

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~~24.~~ The volume control circuitry of claim 23, wherein said first and second storage devices are registers.

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~~25.~~ The volume control circuitry of claim 23, wherein when said incrementor increments or decrements said current value, said increment or decrement is by a value of one.

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~~26.~~ Volume control circuitry for controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer is configured to provide at least one volume component to wavetable data addressed by said synthesizer, comprising:

(a) a memory having first storage locations for storing current values of each one of said at least one volume component, and second storage locations

for storing final values of said each one of said at least one volume component, wherein said final values are directly programmed into said second storage locations;

(b) a comparator coupled to said memory for periodically comparing a current value of a volume component with a final value of said volume component to determine if said current value is less than, greater than, or equal to said final value; and

(c) an incrementor coupled to said comparator and said memory, wherein said incrementor is configured to increment said current value in response to a determination by said comparator that said current value is less than said final value, and configured to decrement said current value in response to a determination by said comparator that said current value is greater than said final value.

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~~27.~~ The volume circuitry of claim 26, wherein said memory is a random access memory, said first storage locations comprise a first column of registers in said random access memory, and said second storage locations comprise a second column of registers in said random access memory.

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~~28.~~ The volume control circuitry of claim 26, wherein when said incrementor increments or decrements said current value, said increment or decrement is by a value of one.

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~~29.~~ The volume control circuitry of claim 27, wherein when said incrementor increments or decrements said current value, said increment or decrement is by a value of one.

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~~30.~~ Volume control circuitry for controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer is configured to provide a volume component to wavetable data addressed by said synthesizer, comprising:

(a) memory means having a first storage location for storing a current value of said volume component, and a second storage location for storing a final value of said volume component, wherein said final value is directly programmed into said second storage location;

(b) comparing means coupled to said memory for periodically comparing said current value with said final value to determine if said current value is less than, greater than, or equal to said final value; and

(c) incrementing means coupled to said comparing means and said memory means for incrementing said current value in response to a determination by said comparing means that said current value is less than said final value, and decrementing said current value in response to a determination by said comparing means that said current value is greater than said final value.

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~~31.~~ Volume control circuitry for controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer interfaces and provides audio enhancement to a host computer of the type including a central processor, and wherein said synthesizer is configured to provide a volume component to a wavetable data addressed by said synthesizer, comprising:

(a) a first storage means for storing a current value of said volume component;

(b) a second storage means for storing a final value of said volume component, wherein said final value is directly programmed into said second storage means by the central processor;

(c) comparing means coupled to said first and second storage means for periodically comparing said current value with said final value to determine if said current value is less than, greater than, or equal to said final value; and

(d) incrementing means coupled to said comparing means and said first storage means for incrementing said current value in response to a determination by said comparing means that said current value is less than

said final value, and decrementing said current value in response to a determination by said comparing means that said current value is greater than said final value.

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~~32.~~ Volume control circuitry for controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer is configured to provide one or more volume components to wavetable data addressed by said synthesizer, comprising:

(a) memory means having first storage locations for storing current values of each volume component, and second storage locations for storing final values of each volume component, wherein said final values are directly programmed into said second storage locations;

(b) comparing means coupled to said memory means for periodically comparing a current value of a volume component with its final value to determine if said current value is less than, greater than, or equal to said final value; and

(c) incrementing means coupled to said comparing means and said memory means for incrementing said current value in response to a determination by said comparing means that said current value is less than said final value, and decrementing said current value in response to a determination by said comparing means that said current value is greater than said final value.

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~~33.~~ A method of controlling volume incrementing in a digital wavetable audio synthesizer, wherein said synthesizer interfaces and provides audio enhancement to a host computer of the type including a central processor, and wherein said synthesizer is configured to provide one or more volume components to wavetable data addressed by said synthesizer, comprising the steps of:

(a) programming a current value of a volume component into a first storage device;

(b) programming a final value of said volume component into a second storage device by the central processor;

(c) reading said current and final values and comparing said values to determine if said current value is less than, greater than, or equal to said final value;

(d) incrementing said current value if said current value is less than said final value, determining said current value if said current value is greater than said final value, or not changing said current value if said current value is equal to said final value;

(e) writing said current value resulting from step (d) in said first storage device; and

(f) periodically repeating steps (c)-(e) unless or until it is determined in step (c) that said current value is equal to said final value.

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~~34.~~ The method of claim 33, wherein said first and second storage devices are registers.

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~~35.~~ The method of claim 34, wherein said registers are a part of a register array.

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~~36.~~ The method of claim 33, further comprising the step of programming said final value into both said first and second storage devices to enable said volume component to be instantly changed to said final value as opposed to incremented or decremented until said final value is reached.

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~~37.~~ The method of claim 33, wherein in step (d), if said current value is incremented or decremented, said increment or decrement is by a value of one.

REMARKS

Claims 20-37 are pending.

Claims 1-~~19~~ 7 have been canceled.

Claims ~~20~~ 8-37 have been added.

The specification has been amended to address certain informalities noted by Applicants. No new matter has been included in the specification by these amendments. Additionally, these amendments are not intended to limit the scope of the claims in any way.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is invited to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231,

on July 6, 1996.

Attorney for Applicants — Date of Signature: 7/6/96

Respectfully submitted,

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